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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,297	10/02/2001	Sean S. Chen	NSC-P05052	9656

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/970,297	CHEN, SEAN S.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,11-13,15-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,11-13,15-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a) because figure 3 fails to show any of the detail of circuit 320 as recited in the specification. Furthermore 320 of Fig. 3 discloses a blank, non-descriptive, box. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-8, 12-13, and 16-21 rejected under 35 U.S.C. 102(b) as being anticipated by Kadanka et al. (USPN 5,621,308).

With respect to claim 1, Kadanka et al discloses in Fig. 2, "a band-gap reference circuit (72 of Fig. 2), comprising:

a band-gap reference unit (52, 53, 55, 56, 58, and 59);

a buffer circuit electronically coupled with said band-gap reference unit (54); and

a single component voltage pull-up device (57) that is separate from said band-gap reference unit (57 is separate from 52, 53, 55, 56, 58, and 59) electronically coupled between said band-gap reference unit and said buffer circuit (57 is electrically coupled to the band-gap unit via its base, and to the buffer 54 via its collector), wherein said voltage pull-up device acts to reduce a required supply voltage to maintain a band-gap reference voltage and wherein said voltage pull-up device is implemented as a transistor (57 acts to reduce a required supply voltage by compensating for the to the current provided by 52 and 53 to load transistors 55 and 56. Since the base of 52 and 53 are both connected to the collector of 55, the collector current of 55 is increased by the sum of the base currents of 52 and 53. To correct this 57 is used to draw twice as

much current as each transistor 52 and 53 (i.e. both 52 and 53 draw Ic/4 and 57 draws Ic/2). Thus 55 will have a current error of Ic/4+Ib/4 (Where Ib is the base current of 52 and 53) and 56 will have a current error of Ic/4-Ib/4. Since 57 draws Ic/2 current the current difference between 55 and 56 will be compensated by 57's current draw which is equal to the error current. This compensation reduces impedance and improves power supply rejection. Thus, a lower supply voltage is capable of being used to supply the band-gap circuit to do 57's compensating abilities.)."

With respect to claim 2, Kadanka et al. discloses, "a band-gap reference circuit as described in Claim 1, wherein said band-gap reference circuit resides in an integrated circuit device (clearly Kadanka et al.'s circuit is resides in an integrated circuit see Col. 1 lines 10-17)."

With respect to claim 3, Kadanka et al. discloses, "a band-gap reference circuit as described in Claim 1, wherein said band-gap reference circuit is implemented in a silicon substrate (clearly Kadanka et al.'s circuit is implemented in a silicon substrate Col. 1 lines 10-17)."

With respect to claim 4, Kadanka et al. discloses, "a band-gap reference circuit as described in Claim 1, wherein said buffer circuit is implemented as a transistor (clearly 54 is a buffer)."

With respect to claim 7, Kadanka et al. discloses in Fig. 2, "an electronic device, comprising:

a silicon substrate (clearly Kadanka et al.'s circuit has a silicon substrate Col. 1 lines 10-17);

electronic circuitry constructed in said silicon substrate (clearly Kadanka et al.'s circuitry is constructed in a silicon substrate Col. 1 lines 10-17);

and a band-gap reference circuit (circuit of Fig. 2) comprising a band gap reference unit (52, 53, 55, 56, 58, and 59), a buffer circuit (54), and a single component voltage pull-up device (57) that is separate from said band-gap reference unit electronically coupled in said electronic device (57 is separate from 52, 53, 55, 56, 58, and 59), wherein said electronic circuitry requires reference to the output voltage of said band-gap reference circuit (57 requires the output current generated at the collector of 53) and said band-gap reference circuit is enabled for low impedance by said buffer circuit (54 controls the band-gap reference unit to operate in low impedance), wherein said buffer circuit comprises a transistor (clearly 54 is a transistor), and wherein said single component voltage pull-up device is coupled between said band-gap reference unit and said buffer circuit (57 is a pull-up transistor coupled between the band-gap reference unit of 52, 53, 55, 56, 58, and 59 and buffer 54 through its base to collector connections)."

With respect to claim 8, Kadanka et al. discloses, "an electronic device as described in Claim 7, wherein said electronic device is an integrated circuit device (clearly Kadanka et al.'s circuit is resides in an integrated circuit see Col. 1 lines 10-17)."

With respect to claim 12, "an electronic device as described in Claim 7, wherein said band-gap reference circuit is enabled for low supply voltage (there is no explicit recited definition of a "low supply voltage". Thus Kadanka et al.'s circuit does operate at a low supply voltage.)."

With respect to claim 13, Kadanka et al. discloses "an electronic device as described in Claim 12, wherein said band-gap reference circuit is enabled for said low supply voltage by a voltage pull-up device (clearly it can be seen in the discussion of claim 2 that pull device 57 allows for low supply voltage operation)."

With respect to claims 16-21, Examiner has considered all of the claim limitations and it can be seen that claims 16-21 essentially recites the method using/composing the circuits of claims 1-4, 7-8, and 12-13 as rejected above. Thus claims 16-21 are rejected for at least the same reasons as claims 1-4, 7-8, and 12-13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadanka et al. (USPN 5,621,308) in view of Mietus (USPN 5,666,046).

Kadanka et al. disclose, in Fig. 2, the circuits of claims 6, 7,13, and 21 (see above rejections). Kadanka et al. does not expressly disclose that transistor 54 (i.e. transistor which provides the band-gap voltage, and the emitter follow buffer) has a "less than 1.0 V_{BE}". However, it is notoriously well known, as expressly taught by

Mietus (e.g., see Col. 1, lines 56-67), to use a transistors that have a V_{BE} voltage of 0.7 volts in a band-gap circuit for the advantage of using a lower supply voltage (e.g., 0.8 volts). Therefore, it would have been obvious for one skilled in the art to manufacture all of the transistors of Kadanka et al. (including transistor 54) with "less than 1.0 V_{BE}" for the expected advantage allowing for a lower supply voltage. One would have been motivated to manufacture all of the transistors of Kadanka et al. (including transistor 54) with "less than 1.0 V_{BE}" to lower the supply voltage thus reducing the amount of power consumed by the circuit of Fig. 2 of Kadanka et al. Thus all the limitations of claims 6, 11, 15 and 23 are disclosed by the above combination.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Capici (USPN 6,118,264) discloses in Fig. 1 a notoriously well-know band-gap reference unit which is composed in the same way as the band-gap reference unit of 52-53,55-56, and 58-59 of Fig. 2 of Kadanka et al.

Response to Arguments

Applicant's arguments filed 30 January 2007 have been fully considered but they are not persuasive.

Applicant argues that claim 1 requires at least requires band-gap reference unit, and a single component voltage pull-up device this is separate from the band-gap reference circuit, and that Kadanka et al. (USPN 5,621,308) does not teach or suggest a band-gate reference circuit and a single component voltage pull-up device that is

separate from the band-gap reference unit. This cannot be found persuasive, first all the limitations of the claims are given the broadest reasonable interpretation and due to the broadest reasonable interpretation the circuit of 52-55, 58, and 59 can be interpreted as a band-gap reference circuit. This is because alone 52-55, 58 and 59 is a circuit composed to output a band-gap voltage (i.e. band-gap voltage connected to the base of 56 output from the above "band-gap reference circuit"). Again see Fig. 1 of Capici which discloses a notoriously well-know band-gap reference unit which is composed in the same way as the band-gap reference unit of 52-53,55-56, and 58-59 of Fig. 2 of Kadanka et al. Second, Kadanka et al. discloses a band-gap circuit connected as similarly recited as Applicant (i.e. bang-gap circuit (52-53,55-56, and 58-59), voltage pull up (57) separate from band-gap reference unit (57, is separate from the band-gap reference unit), and a buffer (54) with the pull-device coupled between the buffer and the band-gap reference unit). Third, it can be seen that Applicant similarly discloses in Fig. 3 a combination of interconnected circuits elements that comprise a band-gap reference circuit. There is no distinction between each of the separate band-gap reference unit, buffer, and voltage pull up device. Therefore if Kadanka et al. does not disclose "separate circuits" Applicant's circuit also fails to disclose a "separate" voltage pull-up device, since all of the circuit elements of Fig. 3 are connected together.

Applicant further argues that Kadanka et al. fails to disclose, the band-gap reference unit residing in an integrated circuit device, "implemented on a silicon substrate, and "said buffer circuit is implemented as a transistor." These arguments cannot be found persuasive, again see Col. 1 lines 12-17, which discloses the band-gap reference circuit being composed in an "integrated circuit (IC)" and is "silicon based"

(i.e. having a silicon substrate), also see Col. 4 lines 25-31 which discloses the circuit of Fig. 2 being fabricated similarly to Fig. 1. Furthermore it can clearly be seen that 54 is a transistor and a buffer (i.e. emitter-follower). Thus Applicant's arguments cannot be found persuasive and all of the above rejections are maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
April 2, 2007

Kenneth B. Wells
Primary Examiner